

LIST OF REFERENCES CITED BY APPLICANT (Use several sheets if necessary)	ATTY DOCKET NO. 9818-093-999	APPLICATION NO To be assigned
	APPLICANT REESE et al.	
	FILING DATE Herewith	GROUP To be assigned

## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
ah	5,811,857	09/22/1998	Assaderaghi et al.	—	—	—
ah	6,034,397	03/07/2000	Voldman	—	—	—
ah	6,404,269 B1	06/11/2002	Voldman	—	—	—

## FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
					YES NO

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

ah	Amerasekera et al., "ESD in Silicon Integrated Circuits", Second Edition, John Wiley & Sons, Ltd., 2002, pp. 200-206, 215-216
	Anderson and Krakauer, "ESD protection for mixed-voltage I/O using NMOS transistors stacked in a cascode configuration", Microelectronics Reliability, 39, 1999, pp. 1521-1529
	Duvvury et al., "ESD Design For Deep Submicron SOI Technology", Symposium on VLSI Technology Digest of Technical Papers, 1996, pp. 194-195
	Verhaege et al., "The ESD Protection Capability of SOI Snapback NMOSFETS: Mechanisms and Failure Modes", EOS/ESD Symposium, 1993, pp. 215-219
	Voldman et al., "Electrostatic Discharge Characterization of Epitaxial-Base Silicon-Germanium Heterojunction Bipolar Transistors", EOS/ESD Symposium, 2000, pp. 239-250
	Voldman et al., "Electrostatic Discharge (ESD) Protection in Silicon-on-Insulator (SOI) CMOS Technology with Aluminum and Copper Interconnects in Advanced Microprocessor Semiconductor Chips", EOS/ESD Symposium, 1999, pp. 105-115
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EXAMINER



DATE CONSIDERED

02/14/05

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.